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Resonant DC/DC Converter to Reduce Voltage Stress and Ripples

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***Abstract*: This project proposes a novel method to reduce voltage stresses across switches (IGBT), transformer windings and to reduce the output voltage ripple. Circuit sharing technique is used to reduce the stresses across the transformer windings. Multilevel converter technique is used to reduce the voltage stress across the switches. The switches are turned on using ZVS scheme to reduce stresses further. The current doubler rectifier used to reduce output ripple current which further increases the efficiency. We use phase shift pwm method to turn on and off the switches.**

***Keywords*- Phase shift pulse width modulation, Resonant converter, voltage stress reduction.**

I. Introduction

The prime motive of any drive is to extract maximum output from the system. That is to increase the efficiency of the system. The efficiency of any system is directly dependent on losses. There are some losses in the system which always goes unnoticed. The losses in switches and transformer windings due to voltage stress are such losses. The proposed topology is to reduce such losses and reduce the ripples in output current. This makes the system very reliable and effective.

The voltage stress of power switches in the N-level converters/inverters is equal to Vin / (N−1). In order to meet the demand of high efficiency, small-volume, and lightweight converters, active clamped converters[5], asymmetric half-bridge converters, series resonant converters[2], and phase-shift full-bridge converters have been developed to achieve zero-current switching (ZCS)[1][3][10] at turn-off or zero-voltage switching (ZVS)[3][4][5][9] at turn-on. In the secondary side, the center tapped rectifier can be used to regulate output voltage, smooth the output ripple current, and have one diode voltage drop. The voltage stress of rectifier diodes in the diode bridge rectifier[6] is much lower compared with that in centre tapped rectifier.

A new soft-switching pv input[8][6] dc/dc resonant converter[7] for high-voltage applications is presented in this paper. A three-level diode-clamped[5] dc/dc converter[7][12] with one flying capacitor[11] is adopted to reduce the voltage stress of active switches at one-half of the input voltage. The phase shift PWM scheme is used to regulate the output voltage at the desired voltage level. Current doubler rectifiers are adopted in the secondary side to reduce the output ripple current.

II. Circuit configuration

The proposed ZVS dc/dc converter is shown in fig.1. The capacitive input voltage divider will divide the input voltage Vin to vCin1 =vCin2 = Vin/2. S1-S4 are IGBT with voltage stresses Vin/2. C1 and C2 are dc blocking capacitance and Lr1 and Lr2 are resonant inductance. T1 and T2 are the transformers. D1-D4 are rectifier diodes. The proposed converter adopts phase shift PWM strategy to regulate output voltage.

There are two three level PWM circuits in proposed converter. These two circuits use same

power switches S1-S4, the flying capacitor Cf, and the clamped diodes Da and Db. Three voltage levels Vin, Vin/2 and zero are generated at AC terminals.

Current doubler rectifier are used at the secondary side to obtain stable output voltage with one diode conduction loss and partially cancel output ripple current. The input to the current divider is given from a photovoltaic system[6] which consists of pv cell array and a boost converter.

The two circuits at the primary side uses same power switches S1-S4. The component of first circuit include Cin1, Cin2, Da, Db, Cf, S1-S4, Cr1-Cr4, C1, Lr1, T1, D1, D2, Lo1 and Lo2.

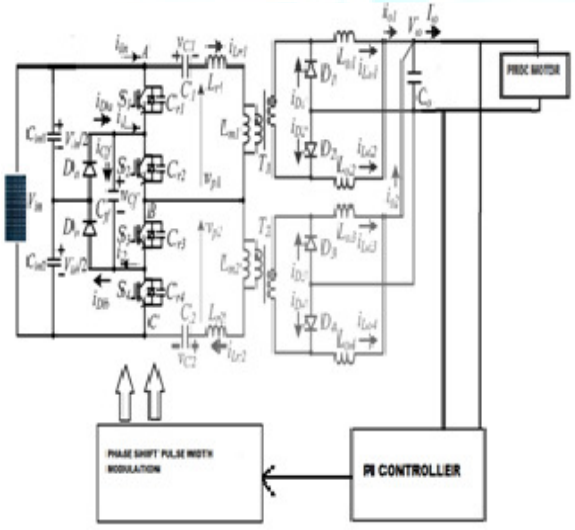

Fig 1: zvs dc/dc converter feeding PMDC motor

The second circuit consist of Cin1, Cin2, Da, Db, Cf, S1-S4, Cr1-Cr4, C2, Lr2, T2, D3, D4, Lo3 and Lo4.

The circuit diagram of the DC to DC resonant converter fed PMDC motor is shown above. Here the resonant converter is the key part, output from converter is effectively utilized for driving a PMDC motor, and motor controlling is done with the help of a PI controller.

The circuit consists of a dc power source along with voltage divider and multilevel inverter in the primary circuit. The secondary side consists of rectifier stage. The input dc source is a PV input which is followed by a capacitive potential divider.

The input capacitors Cin1 and Cin2 divide the voltage and will feed to the multilevel inverter. The multilevel inverter consists of four IGBT switches. The multilevel inverter are used for two purposes.

a) To reduce the voltage across each input switch
b) To convert the dc power to ac power

III. Operating principle

The following assumptions are made to simplify the system analysis.

1) Power semiconductors S1–S4, D1–D4, Da, and Db are ideal.

2) Lm1 = Lm2 = Lm, Lr1 = Lr2 = Lr Lm, and Lo1 = Lo2 = Lo3 = Lo4 = Lo.

3) Cin1 andCin2 are equal and large enough to be considered as two voltage sources VCin1 = VCin2 = Vin/2.

4) The turn ratio of transformers T1 and T2 is

n = np/ns.

5) Cr1 = Cr2 = Cr3 = Cr4 = Cr.

6) C1, C2, and Cf are large enough to be treated as three constant voltages VC1 = VC2 = VCf = Vin/2.

7) Co is large enough to be considered as a constant output voltage

MODES OF OPERATION

MODE 1

S1 is turned off. Since Lo1-Lo4 are large enough, primary side currents are almost constant in mode 1. Switch S1 is turned off at ZVS. ZVS turn on condition of S4 is done. If the ZVS turn-on condition of S4 is met voltage across S4 can be decreased to zero voltage.

MODE 2

In mode 2, Vab=Vbc=(Vin)/2 and vpi=vp2=0. Thus primary and secondary winding voltages are all zero. D1-D4 are forced to conduct, and the output inductor voltages VLo1=VLo2=VLo3=VLo4= -Vo. ILo1-ILo4 all decrease with current slope –Vo/Lo in this mode. This mode ends with S2 being turned off

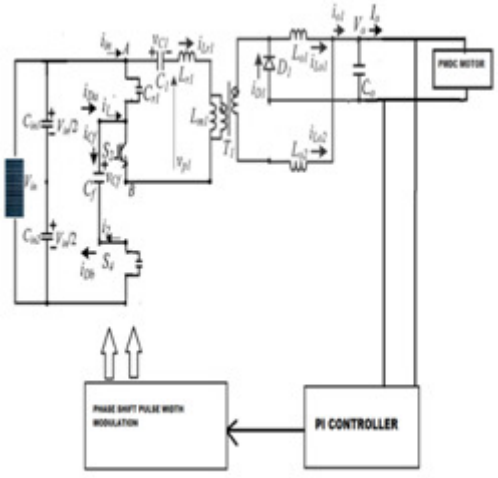

Fig 2: Mode 1

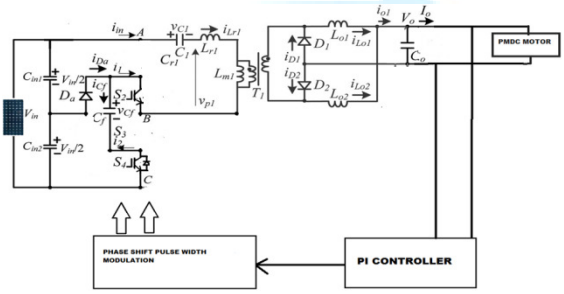

Fig 3: Mode 2

MODE 3

S2 is turned off. Cr2 is charged from zero voltage and Cr3 is discharged linearly from Vin/2. Rising slope of voltage across S2 is limited by Cr2 and Cr3. Then S3 is turned on by ZVS and once this is met Cr3 is discharged to zero voltage

MODE 4

Vcr3 =0 and anti-parallel diode of S3 starts conducting. Vab = Vin, Vbc = 0, Vp1 = Vin/2 and Vp2 = -Vin/2. Since D1-D4 are still conducting primary and secondary windings, all have zero voltage. Inductor current iLr1 increases and iLr2 decreases in this mode. This mode ends when diode current iD1 and iD4 are decreased to zero.

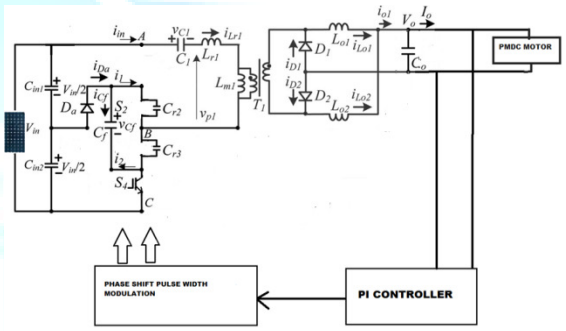

Fig 4: Mode 3

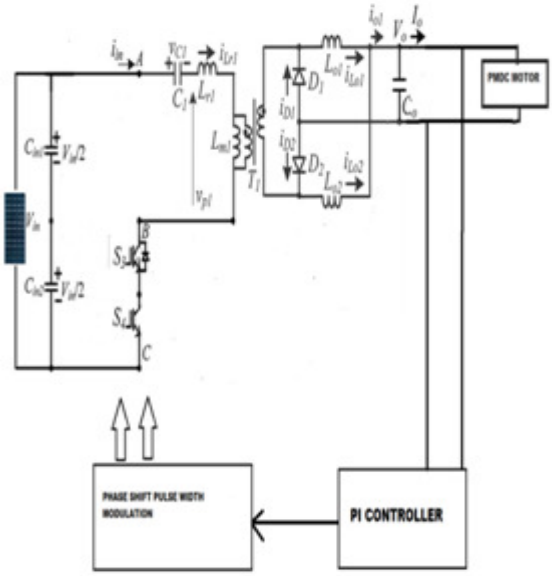

Fig 5: Mode 4

MODE 5

Primary current iLr1 increases linearly with voltage Vin/2 and iLr2 decreases linearly with voltage – Vin/2. The inductor current iLo1 and iLo4 increase and iLo2 and iLo3 decrease in this mode

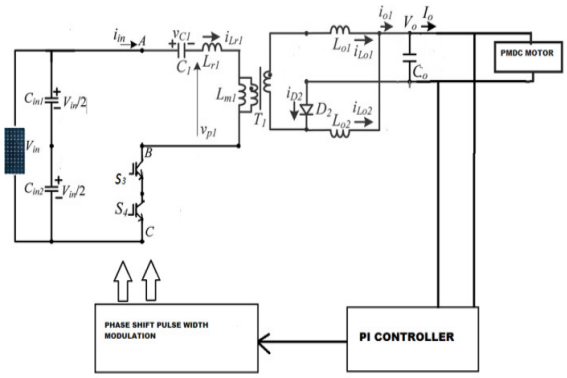

Fig 6: Mode 5

MODE 6

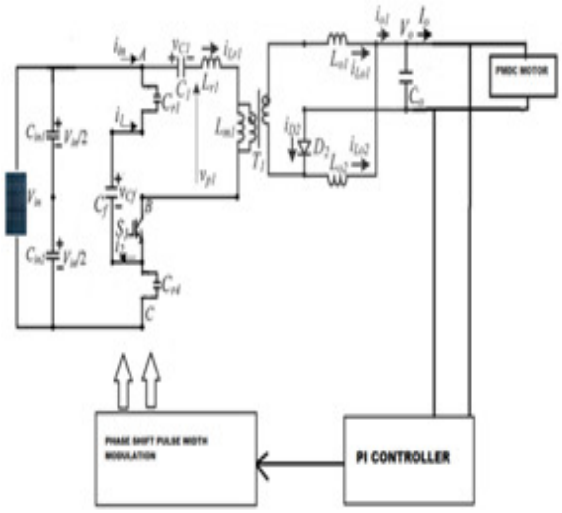

Fig 7: Mode 6

Rising slope of voltage across S4 is limited by Cr1 and Cr4. Thus S4 is turned off at ZVS. Mode ends when Vcr1 = 0 and Vcr4 = Vin/2.

MODE 7

In this mode voltage Vab = Vbc = Vin/2 and Vp1 = Vp2 = 0. Thus D1-D4 are conducting. The output inductor voltages and inductor currents will decrease. Diode currents Id1 and Id4 decrease. This mode ends when S3 is turned off

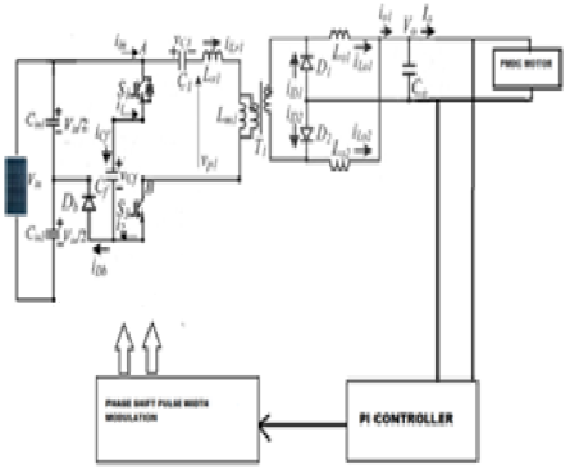

Fig 8: Mode 7

.MODE 8

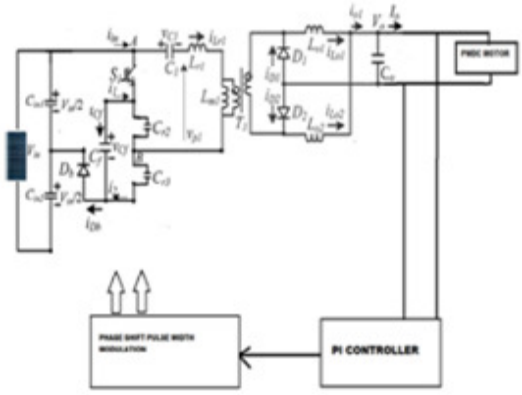

Fig 9: Mode 8

Cr2 is discharged linearly from Vin/2 and Cr3 is charged linearly from zero voltage. The rising slope voltage of S3 is limited by Cr2 and Cr3. Thus S3 is turned off at ZVS. This mode ends when Vcr2 = 0 and Vcr3 = V in/2.

MODE 9

Vab = 0, Vbc = Vin, Vpi = -Vin/2 and Vp2 = Vin/2. Primary and secondary side voltages of T1 and T2 are all zero voltage. This mode ends when Id2 = Id3 = 0.

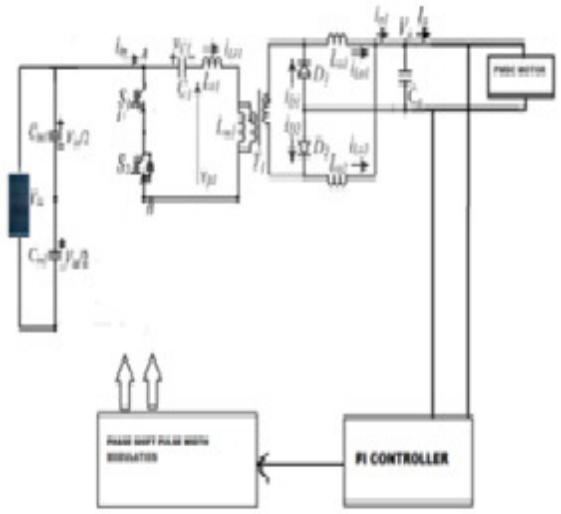

Fig 10: Mode 9

MODE 10

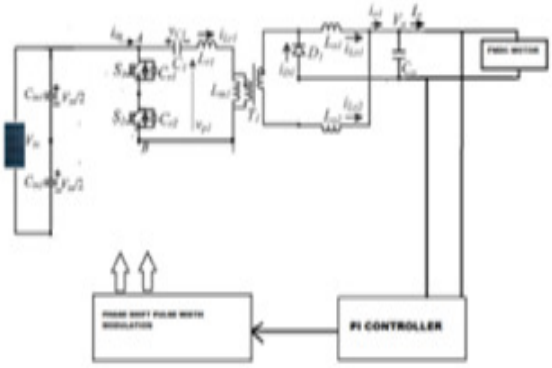

Fig 11: Mode 10

Transformers T1 and T2 are working as forward type transformers. Thus primary current iLr1 decreases linearly with –Vin/2 and iLr2 increases linearly with Vin/2. The inductor current iLo1 and iLo4 decrease and iLo2 and iLo3 increases. This mode ends with S1 is turned off

IV. Experimental results

The proposed circuit was developed and analyzed in MATLAB software. The PV input was given to the multilevel converter through a capacitive voltage divider which in turn gets rectified and feed a PMDC motor.

MATLAB simulation circuit diagram, resultant waveforms for converter output voltage, current and other output waveforms are given below

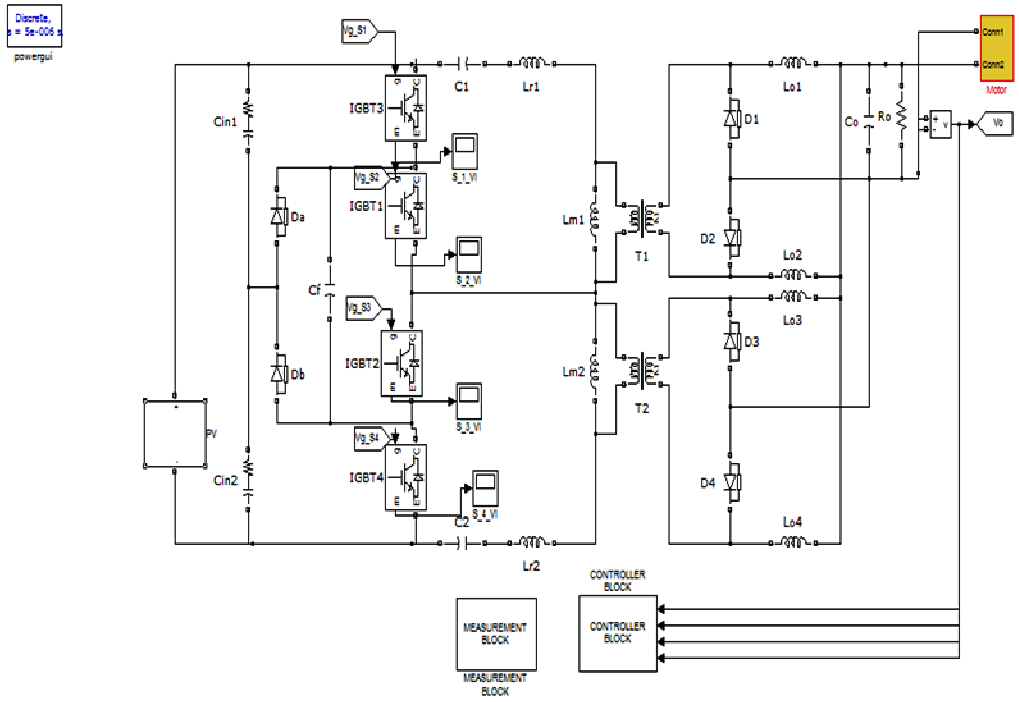

Fig 12: MATLAB simulation circuit.

V. Resultant waveform

The simulation results consist of output voltage waveform, voltage across switch, voltage across primary and secondary windings of transformer voltage across output inductor, current through output inductor and resonant inductor current

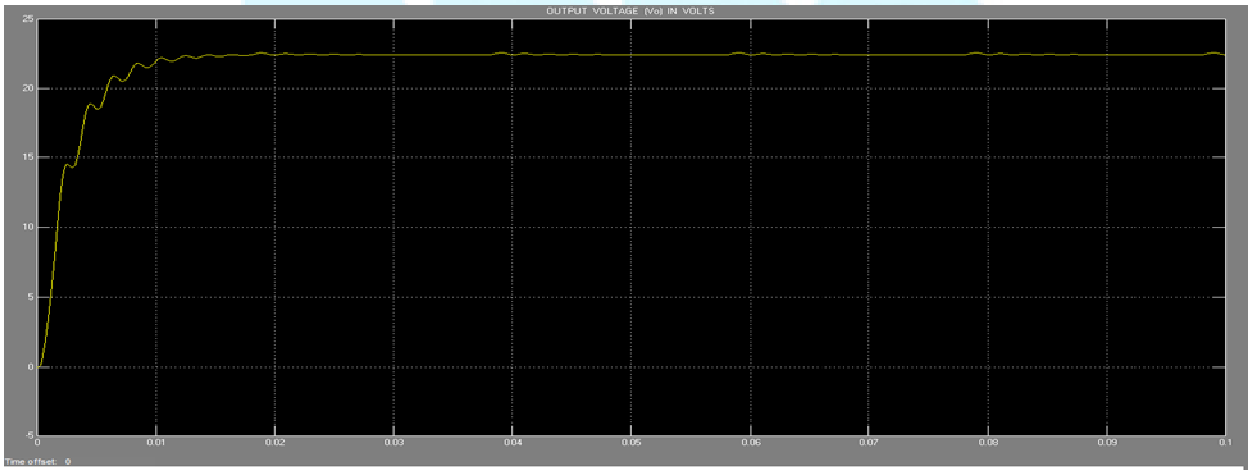

Fig 13 : Output voltage waveform

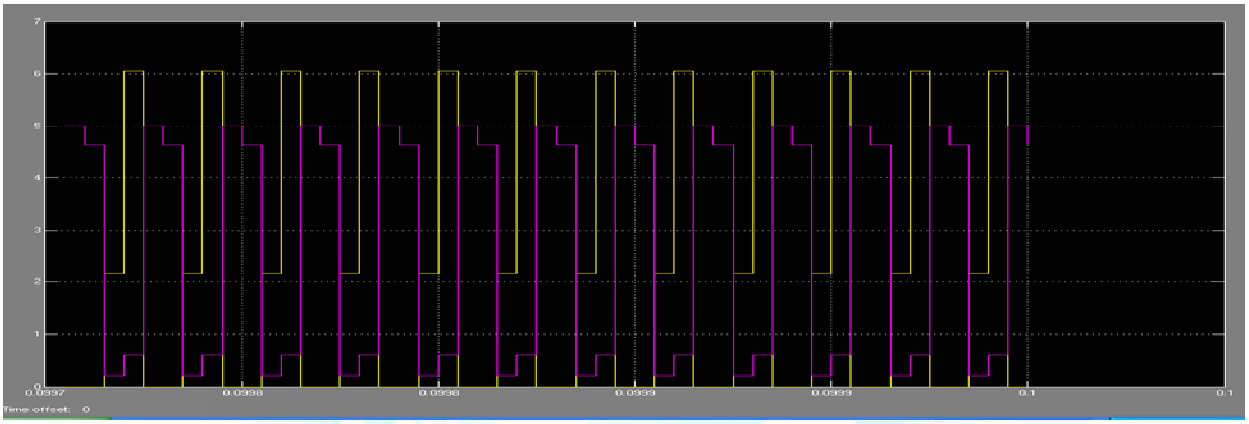

Fig 14: Voltage across switch

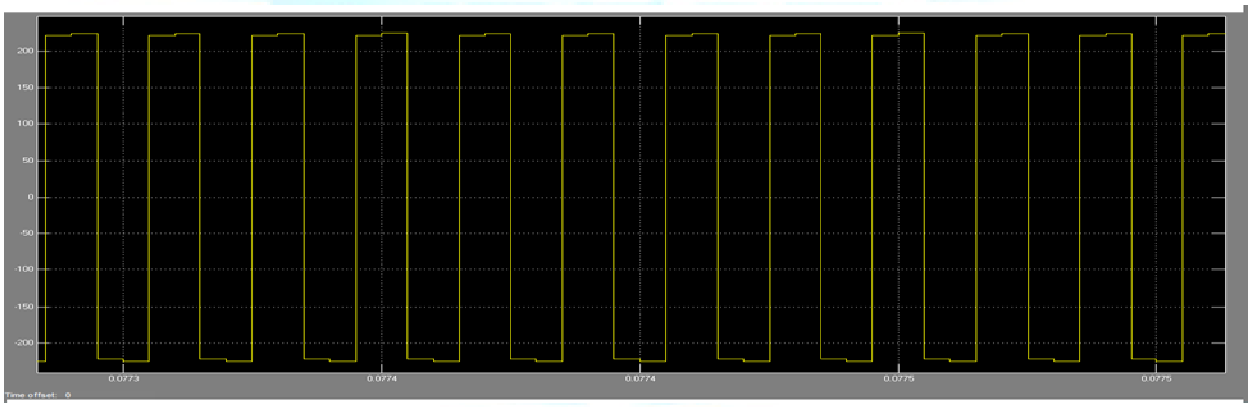

Fig 15: Voltage across transformer primary winding

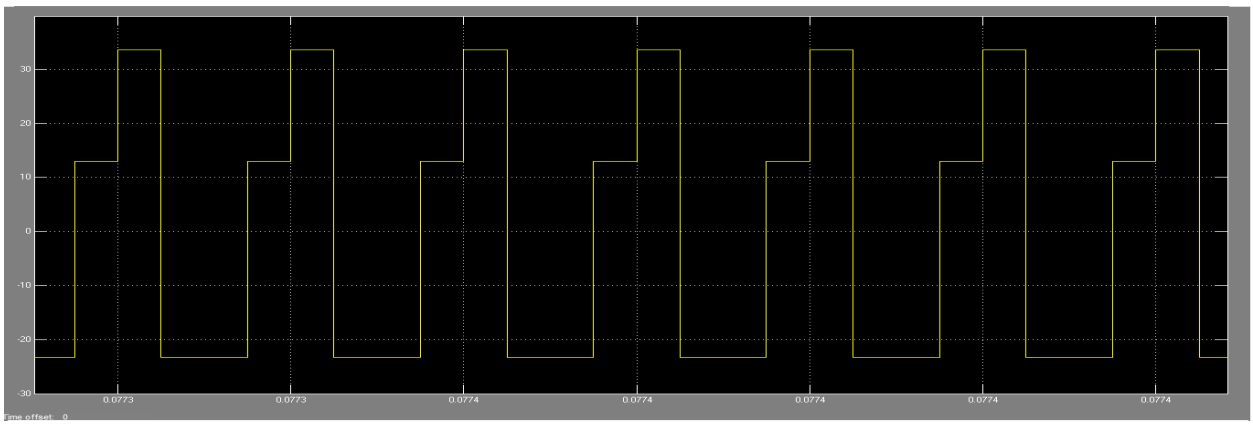

Fig 16 : Voltage across output inductor

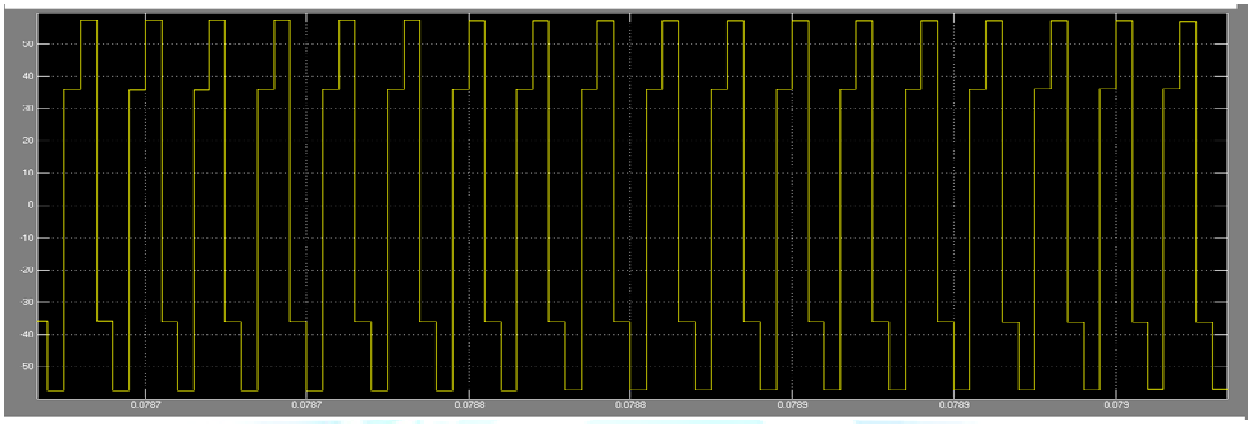

Fig 17 Voltage across secondary winding of transformer

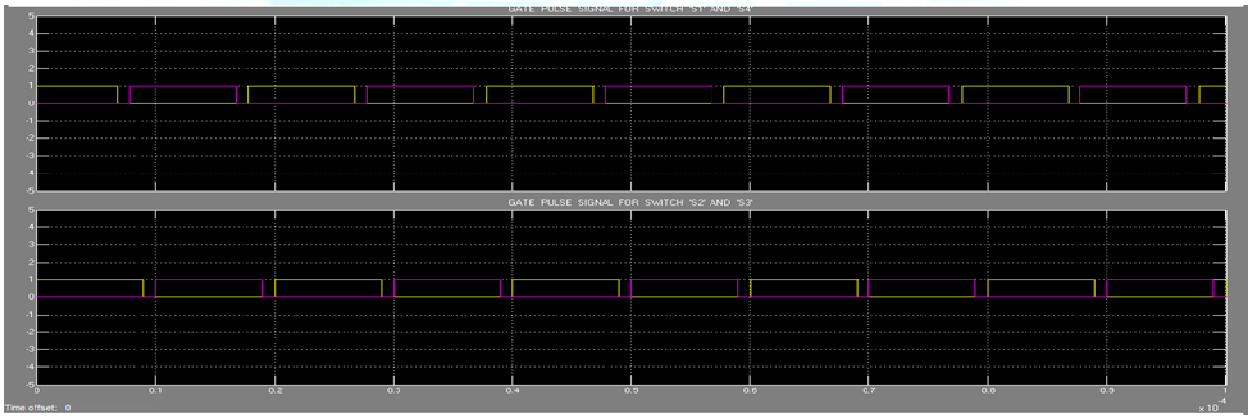

Fig 18 Gate pulse for all switches

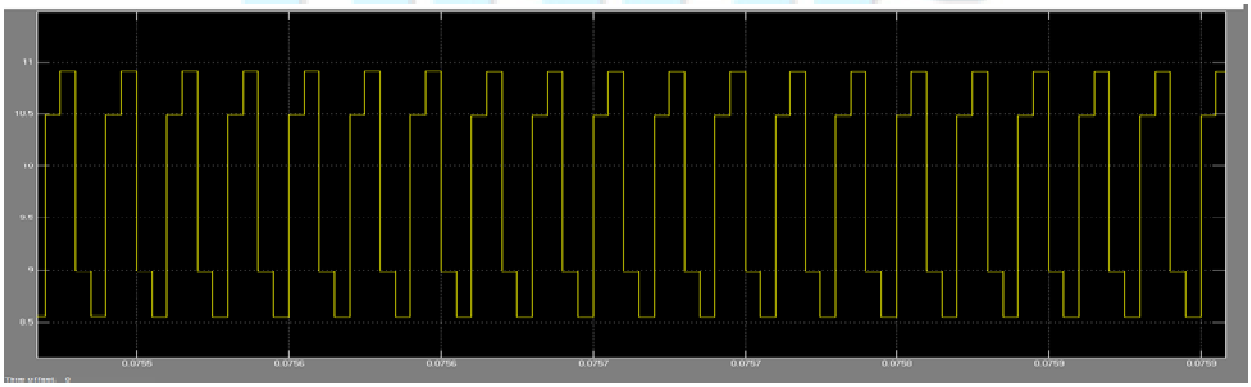

Fig 19 : Current through output indutor

VI. Conclusion

In this paper a converter topology is proposed to reduce the voltage stress across switches and transformer windings and also to reduce the ripple in output current. Phase shift PWM method is used to control the IGBT switches and thus regulate output voltage. Compared to conventional parallel three level dc-dc converter, the proposed technology uses lesser number of switches.

Thus by using the proposed converter topology we can achieve,

a) Lesser voltage stress across IGBT switches.
b) Lesser voltage stress across transformer windings.
c) Low ripples in output current.
d) Better output voltage with greater stability.

Use of lesser number of switch reducing cost and losses

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